INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/DE 99/02523

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06K9/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 791 899 A (HARRIS CORP) 27 August 1997 (1997-08-27) column 6, line 17 - line 50; figures 7-10	1-3
P,A	DE 197 56 560 A (SIEMENS AG) 1 July 1999 (1999-07-01) column 1, line 64 -column 2, line 5	1-3
A	US 4 290 052 A (EICHELBERGER CHARLES W ET AL) 15 September 1981 (1981-09-15) column 4, line 56 -column 5, line 36; figure 2	1-3

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
23 February 2000	01/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Granger, B

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/DE 99/02523

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0791899 A	27-08-1997	US 5963679 A	05-10-1999
		JP 9251530 A	22-09-1997
DE 19756560 A	01-07-1999	NONE	
US 4290052 A	15-09-1981	NONE	

INTERNATIONALER RECHERCHENBERICHT

Internationales Aktenzeichen
PCT/DE 99/02523

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
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Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 7 G06K

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	EP 0 791 899 A (HARRIS CORP) 27. August 1997 (1997-08-27) Spalte 6, Zeile 17 - Zeile 50; Abbildungen 7-10	1-3
P,A	DE 197 56 560 A (SIEMENS AG) 1. Juli 1999 (1999-07-01) Spalte 1, Zeile 64 -Spalte 2, Zeile 5	1-3
A	US 4 290 052 A (EICHELBERGER CHARLES W ET AL) 15. September 1981 (1981-09-15) Spalte 4, Zeile 56 -Spalte 5, Zeile 36; Abbildung 2	1-3

☐ Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

☒ Siehe Anhang Patentfamilie

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23. Februar 2000	01/03/2000

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Granger, B

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INTERNATIONALER RECHERCHENBERICHT

Angaben zu Veröffentlichu..gen, die zur selben Patentfamilie gehören

Inte   onales Aktenzeichen
PCT/DE 99/02523

Im Recherchenbericht angeführtes Patentdokument	Datum der Veröffentlichung	Mitglied(er) der Patentfamilie	Datum der Veröffentlichung
EP 0791899 A	27-08-1997	US 5963679 A JP 9251530 A	05-10-1999 22-09-1997
DE 19756560 A	01-07-1999	KEINE	
US 4290052 A	15-09-1981	KEINE	

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XP-000856844 P.D. 1998 P. 284-285 (2)

SA 17.7: A Robust, 1.8V 250µW Direct-Contact 500dpi Fingerprint Sensor

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Fingerprints are finding increasing application in commercial authentication. A number of technologies have been applied to fingerprint acquisition including optical, thermal, pressure, ultrasonic and capacitive imaging [1, 2, 3]. Low power, low cost, small size and solid-state integration make capacitive sensing attractive for portable/desktop applications. A recently-reported single-chip capacitive fingerprint sensor uses standard digital CMOS processing [4]. That work focuses on sensor circuit design and does not address issues that arise when operating an exposed silicon die as a human contact sensor.

This high-resolution, low-power direct-contact capacitive sensor using standard CMOS front-end processing exhibits high sensitivity while maintaining an effective barrier to chemical, physical and electrostatic intrusion. The sensor uses direct finger contact with the surface of the sensor IC to capture a capacitive fingerprint image. The sensor consists of a 2-D array of metal plates capped with a thin dielectric layer. Unlike previous designs, each sensing site uses one metal sensor plate [4]. Each functions as capacitor bottom plate, with the finger surface acting as the grounded top plate. Distance between the finger and the sensor and hence the measured capacitance varies with the pattern of ridges and valleys in the fingerprint. The capacitance is "measured" as the change in voltage that results when a fixed charge is removed from each sensing plate.

Figure 1 shows an individual sensing cell with associated column readout circuit. At the beginning of a sensing cycle, each sensor plate is activated using row enable signals RE and RAD and precharged using PRE. Voltage on the sensor node is buffered by source follower, T_2, and gated onto a column data bus, COL, by row select signal RAD. Precharge voltage, V_A, is stored on capacitor C_A by pulsing SHA. Once PRE is released a current source, I_S, drains charge from the plate for a fixed time interval. Change in voltage on the plate is inversely proportional to the capacitance that, in turn, is approximately inversely proportional to the distance of the finger from the surface of the chip. This new voltage, V_B, is stored on capacitor C_B by pulsing SHB. Sensor row access timing is shown in Figure 2. Subsequent circuitry subtracts V_B from V_A to remove pattern noise caused by variations in the threshold voltage of transistors T_1 and T_2 and produce an output approximately proportional to the distance of the finger from the chip. This simple single-plate structure with minimal active circuitry leads to high resolution with high electrical reliability and yield over a large die area.

Choice of dielectric material and thickness is critical in the design of a sensor which must exhibit high sensitivity and yet be resistant to chemical contamination, electrostatic discharge and physical scratching of the surface. Of particular importance are the dielectric layers immediately above and below the sensor plate as shown in Figure 3. The image sensitivity/contrast is proportional to the ratio C_r/C_p where C_r is the capacitance measured when the finger is in contact with the chip surface (ridge capacitance) and C_p is the parasitic capacitance associated with each sensor plate. Altering thickness, dielectric constant, and composition of these two dielectrics achieves high mechanical strength and a chemical barrier while maintaining a high C_r/C_p ratio. This leads to high-contrast images and easier operation at low voltage/low power.

The top dielectric, D1, is a 5000A layer of high-density silicon nitride, a mechanically strong material with a dielectric constant > 7 and a mechanical hardness >3000kg/mm². Silicon nitride also provides a barrier to the entry of water, skin oil and chloride ions. The lower dielectric, D2, is a 1µm layer of P-glass with dielectric constant <3.5 that provides a significant chemical barrier to alkali ions. The combination of these two materials in conjunction with existing front-end process dielectrics gives a C_r/C_p ratio of >10. This combination of dielectric materials is tested by placing samples in boiling NaCl solution for one hour with no surface corrosion detected. Alkali ion retardation has been similarly verified at 200°C with concentrations $>10^{14}/cm^2$.

Electrostatic discharge (ESD) protection is provided by a number of techniques. First, diodes, associated with the RE gated switch, connect to each sensing node. In conjunction with a resistive path from the sensor plate to the switch, these diodes provide limited over-voltage path to VSS or VDD. Second, each sensor plate is surrounded by a grid of top layer metal routing connected to VSS. In operation, additional external techniques may be employed to ensure that the finger is properly discharged before contact with the sensor surface.

A sensor array of 300x300 elements has been fabricated using a standard digital 0.5µm CMOS process with modified final dielectric layers as described previously. A block diagram of the chip is shown in Figure 4. Sensor elements are 50x50µm with over 60% of the sensor area devoted to the sensing plate. The array occupies 15x15mm² yielding a 500dpi image. An external 1µA reference current biases the sensor current sources. A row/column hierarchy of current mirrors distributes this current reference to improve tolerance to isolated manufacturing faults. Sensor integration time is around 1µs. Row read-out can be completed in 50µs. Complete images can be read up to 60Frames/s. Standby power dissipation (when no finger is touching the chip) at 1.8V is 110µW. Active power dissipation (when a finger is present) is 250µW at 60Frames/s. This can be reduced by reducing the imaging frame rate. This compares to 600µW (at 10Frames/s) of previous capacitive sensors and the 2-3W dissipated by commercial optical systems [4]. Performance is summarized in Figure 5. A die micrograph is shown in Figure 7.

A fingerprint image captured by the device is shown in Figure 6. Tests with commercial fingerprint recognition software yield false accept ratios of <1% over a large standard fingerprint database. This compares favorably with results obtained from the same software using commercial optical sensors. Much of the pattern noise evident in Figure 6 is ignored by the recognition software. Similarly, the software works well in the presence of isolated non-functioning pixels. A non-functioning row or column does not significantly affect recognition accuracy. This allows high effective yields even with chip area >200mm².

Acknowledgments:

The authors thank Veridicom for seeing this IC into a product.

References:

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[3] Tsikos, "Capacitive Fingerprint Sensor," US Patent 4353056, Oct., 5, 1982.
[4] Tartagni, Guerrieri, "A 390dpi Live Fingerprint Imager Based on Feedback Capacitive Sensing Scheme," ISSCC Digest of Technical Papers, Feb., 1997.

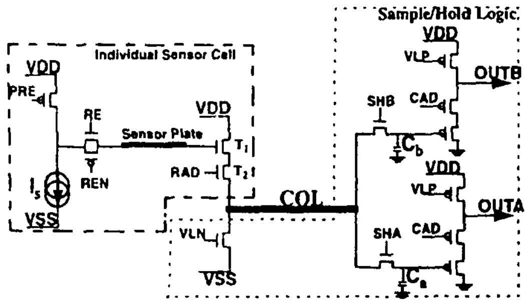

Figure 1: Sensor cell with sample/hold logic.

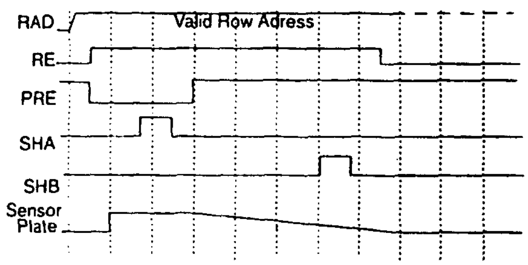

Figure 2: Sensor row access timing.

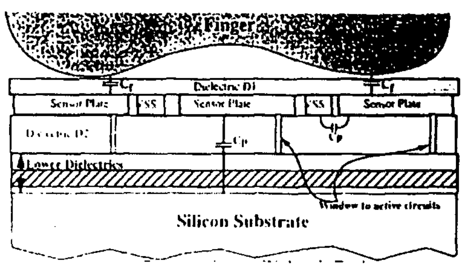

Figure 3: Sensor dielectric design.

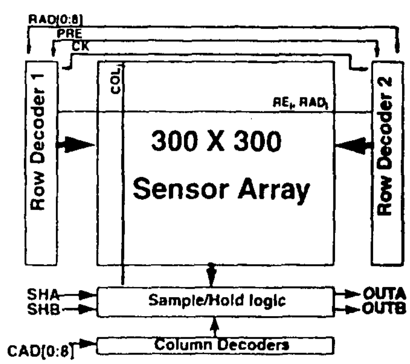

Figure 4: Chip block diagram.

500dpi Direct Contact Fingerprint Sensor

Die Size - 16.5mm X 15.5mm

Technology - 0.5µm, 3.3V, 3LM Digital CMOS

Sensor pitch - 50µm X 50µm

Array size - 300 X 300 sensors

Device count - 582K transistors

Resolution - 500dpi

Power - 250µW @ 1.8V and 60frm/s.

Figure 5: Chip performance summary.

Figure 6: Unprocessed fingerprint image.

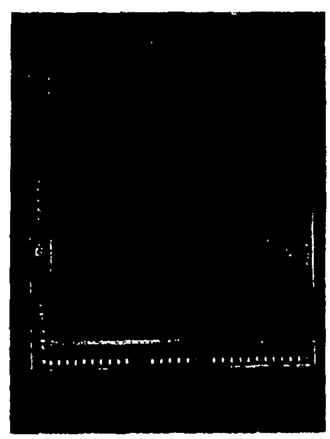

Figure 7: Die micrograph.

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Applic. #

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